	L #	Hits	Search Text	DBs
1	L1	879	(differ$4 near5 (memory storage) near5 (type class)) near10 access$3	USPAT; US-PGPUB
2	L3	84	(differ$4 near5 (memory storage) near5 (type class)) near10 access$3	EPO; JPO; DERWENT; IBM_TDB
3	L6	0	(decod$3 near10 (instruction command)) near50 3	EPO; JPO; DERWENT; IBM_TDB
4	L5	2	(decod$3 near10 (instruction command)) near50 1	USPAT; US-PGPUB
5	L7	8	(differ$4 near5 (memory storage) near5 (type class)) near50 (decod$3 near10 (instruction command))	USPAT; US-PGPUB
6	L8	33	((memory storage) near5 (type class)) near10 access$3 near50 (decod$3 near10 (instruction command))	USPAT; US-PGPUB
7	L9	11	((memory storage) near5 (type class)) near10 access$3 near50 (decod$3 near10 (instruction command))	EPO; JPO; DERWENT; IBM_TDB
8	L10	27	(memory storage) near5 type near50 (decod$3 near10 (instruction command) near20 (modifi$5 alter$3 chang$3 select$5))	USPAT; US-PGPUB
9	L11	9	(memory storage) near5 type near50 (decod$3 near10 (instruction command) near20 (modifi$5 alter$3 chang$3 select$5))	EPO; JPO; DERWENT; IBM_TDB

	L #	Hits	Search Text	DBs
1	L1	879	(differ$4 near5 (memory storage) near5 (type class)) near10 access$3	USPAT; US-PGPUB
2	L3	84	(differ$4 near5 (memory storage) near5 (type class)) near10 access$3	EPO; JPO; DERWENT; IBM_TDB
3	L6	0	(decod$3 near10 (instruction command)) near50 3	EPO; JPO; DERWENT; IBM_TDB
4	L5	2	(decod$3 near10 (instruction command)) near50 1	USPAT; US-PGPUB
5	L7	8	(differ$4 near5 (memory storage) near5 (type class)) near50 (decod$3 near10 (instruction command))	USPAT; US-PGPUB
6	L8	33	((memory storage) near5 (type class)) near10 access$3 near50 (decod$3 near10 (instruction command))	USPAT; US-PGPUB
7	L9	11	((memory storage) near5 (type class)) near10 access$3 near50 (decod$3 near10 (instruction command))	EPO; JPO; DERWENT; IBM_TDB
8	L10	27	(memory storage) near5 type near50 (decod$3 near10 (instruction command) near20 (modifi$5 alter$3 chang$3 select$5))	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20030 12327 0 A1	☐	Content addressable memory with configurable class-based storage partition	365/49
2	US 20020 07571 4 A1	☐	Content addressable memory with configurable class-based storage partition	365/49
3	US 20020 04043 0 A1	☐	Microcontroller	712/234
4	US 65423 91 B2	☐	Content addressable memory with configurable class-based storage partition	365/49
5	US 63381 08 B1	☐	Coprocessor-integrated packet-type memory LSI, packet-type memory/coprocessor bus, and control method thereof	710/110
6	US 60498 97 A	☐	Multiple segment register use with different operand size	714/53
7	US 59499 96 A	☐	Processor having a variable number of stages in a pipeline	712/244
8	US 59182 42 A	☐	General-purpose customizable memory controller	711/5
9	US 58322 58 A	☐	Digital signal processor and associated method for conditional data operation with no condition code update	712/226
10	US 58227 57 A	☐	Computer system with multi-buffer data cache for prefetching data having different temporal and spatial localities	711/129
11	US 57746 81 A	☐	Method and apparatus for controlling a response timing of a target ready signal on a PCI bridge	710/306
12	US 57519 96 A	☐	Method and apparatus for processing memory-type information within a microprocessor	711/145
13	US 57064 59 A	☐	Processor having a variable number of stages in a pipeline	712/200
14	US 57014 37 A	☐	Dual-memory managing apparatus and method including prioritization of backup and update operations	711/162
15	US 56385 24 A	☐	Digital signal processor and method for executing DSP and RISC class instructions defining identical data processing or data transfer operations	712/221
16	US 55772 16 A	☐	Controlling process for a controlling apparatus having a CPU and special function units	712/200
17	US 55724 79 A	☐	Semiconductor integrated circuit having a synchronous type memory	365/230 .06
18	US 52768 89 A	☐	Microprocessor having built-in synchronous memory with power-saving feature	713/322
19	US 52108 41 A	☐	External memory accessing system	711/3
20	US 52108 32 A	☐	Multiple domain emulation system with separate domain facilities which tests for emulated instruction exceptions before completion of operand fetch cycle	712/227
21	US 51971 41 A	☐	Software controlled method of issuing hardware control commands to memory controller from prefetch unit by combining request code and address specified in program instructions	712/205
22	US 49127 07 A	☐	Checkpoint retry mechanism	714/17

	Document ID	U	Title	Current OR
23	US 4908751 A	☐	Parallel data processor	712/12
24	US 4785392 A	☐	Addressing multiple storage spaces	712/227
25	US 4707849 A	☐	High speed automatic test apparatus especially for electronic directory terminals	379/28
26	US 4674063 A	☐	Information processing apparatus having a sequence control function	712/234
27	US 4481570 A	☐	Automatic multi-banking of memory for microprocessors	711/5
28	US 4447876 A	☐	Emulator control sequencer	703/26
29	US 4400772 A	☐	Method and apparatus for direct memory access in a data processing system	710/22
30	US 4325120 A	☐	Data processing system	711/202
31	US 4104719 A	☐	Multi-access memory module for data processing systems	711/150
32	US 4075686 A	☐	Input/output cache system including bypass capability	711/138
33	US 3753234 A	☐	MULTICOMPUTER SYSTEM WITH SIMULTANEOUS DATA INTERCHANGE BETWEEN COMPUTERS	709/253

	Document ID	U	Title	Current OR
1	JP 20030 59263 A	☐	DECODER AND DECODING METHOD OF INSTRUCTION WORD TO BE USED FOR SEMICONDUCTOR MEMORY DEVICE	
2	JP 09044 404 A	☐	MANUFACTURE OF CACHE MEMORY DEVICE AND THE CACHE MEMORY DEVICE	
3	JP 63030 966 A	☐	INFORMATION PROCESSOR	
4	JP 58142 447 A	☐	DATA PROCESSOR	
5	JP 20011 43467 A	☐	Semiconductor memory e.g. multibank type synchronous dynamic random access memory, forwards control signal to memory blocks to execute access commands based on the output of decoder	
6	US 60498 97 A	☐	Segment limit violations checking apparatus for memory access in microprocessor, executes limit generation microcode produced by instruction decoder, to generate limits	
7	US 59110 57 A	☐	Instruction scheduling method in superscalar microprocessor	
8	US 54407 14 A	☐	Decoding system for access to register file with overlapping windows - decoding data accessing instruction for accessing data stored in registers of different types including global, local, input and output type, and catalogued into windows arranged in predefined window sequence	
9	EP 52057 2 A	☐	Data processing appts. - uses single instruction with FIFO buffer to distribute operating codes to multiple processors	
10	EP 35528 6 A	☐	Checkpoint retry mechanism for data processing system - updates addresses automatically to enable retry of instruction sequences in response to error detection since passage of current checkpoint	
11	EP 10795 2 A	☐	Data processor with instruction control system - is controlled by microprogram using two types of operand instruction formats and has improved execution speed	